Amendments to the Claims:

A clean version of the entire set of pending claims (Including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An erasable and programmable non-volatile cell, comprising:

- a first transistor having a source, a drain and a gate;
- a floating capacitor having a floating gate and a control gate, said floating gate being connected to said gate of said first transistor; and
- circuitry for detecting the state, whether erased or programmed, of the cell[[;]],

wherein said circuitry for detecting the state of the cell comprises a second transistor having a source, a drain and a gate, said second transistor being complementary to said first transistor and said gate of said second transistor being connected to said floating gate~~; said floating gate and the gates of said first and second transistors are embodied as single polymer layer~~, and

wherein the drain of the first transistor and the drain of the second transistor are electrically separated from each other such that drain currents of the first and second transistors can be determined separately from each other.

2. (Previously Presented) The cell according to claim 1, ~~characterized in that~~wherein said first transistor is an n-channel transistor and said second transistor is a p-channel transistor.

3. (Currently Amended) The cell according to claim 2, ~~characterized in that~~wherein said first and second transistors are MOSFET transistors.

4. (Currently Amended) ~~The cell according to claim 1, characterized in that the~~ An

erasable and programmable non-volatile cell, comprising:

an n-channel transistor having a source, a drain and a gate;

a floating capacitor having a floating gate and a control gate, said floating gate being connected to said gate of said n-channel transistor; and

circuitry for detecting the state, whether erased or programmed, of the cell,

wherein said circuitry for detecting the state of the cell comprises a p-channel transistor having a source, a drain and a gate, said p-channel transistor being complementary to said n-channel transistor and said gate of said p-channel transistor being connected to said floating gate

wherein an n-well diffusion region of said p-channel transistor is the control gate of said floating capacitor.

5-8. (Canceled)

9. (New) The cell of claim 1, wherein the floating gate and the gates of the first and second transistors are embodied as a single polymer layer.

10. (New) An erasable and programmable non-volatile cell, comprising:

an n-channel transistor having a gate, a source, and a drain;

a p-channel transistor having a gate, a source, and a drain;

a floating capacitor having a floating gate and a control gate, wherein the floating gate is connected to the gate of the n-channel transistor;

wherein the n-channel transistor is adapted to program a data value into the cell by having appropriate programming voltages applied to its gate, source and drain, and

wherein the p-channel transistor is adapted to read the data value from the cell by having appropriate read voltages applied to its gate, source and drain.

11. (New) The cell of claim 11, wherein the drain of the p-channel transistor is adapted to float when the data value is programmed into the cell, and wherein the

drain of the n-channel transistor is adapted to float when the data value is read from the cell.

12. (New) The cell of claim 11, wherein an n-well diffusion region of the p-channel transistor is the control gate of said floating capacitor.

13. (New) The cell of claim 11, wherein the floating gate and the gates of the n-channel and p-channel transistors are embodied as a single polymer layer.